REMARKS

Claim Rejections Under 35 USC 103(a)

Claims 25-29, 52 and 53 have been rejected under 35 USC 103(a) as being unpatentable over Hembree et al. (US Patent No. 5,783,461) in view of Frankeny et al. (US Patent No. 5,065,227) and Pedder (US Patent No. 5,717,245).

Claims 30-34 and 47-51 have been rejected under 35 USC 103(a) as being unpatentable over Hembree et al. (US Patent No. 5,783,461) in view of Frankeny et al. (US Patent No. 5,065,227) and Pedder (US Patent No. 5,717,245).

Claims 35-39 have been rejected under 35 USC 103(a) as being unpatentable over Hembree et al. (US Patent No. 5,783,461) in view of Frankeny et al. (US Patent No. 5,065,227) and Pedder (US Patent No. 5,717,245).

The rejections under 35 USC §103 are respectfully traversed for the reasons to follow.

Summary of the Invention

Claims 25-39 and 47-53 are directed to a "semiconductor component". In the elected embodiment of Figures 1-7, the component can comprise a chip module 24 (Figure 2E), a multi chip module 28 (Figure 3) or a semiconductor package 72 (Figure 7). In each case, the component includes a substrate 10 (Figure 2) and a blanket deposited conductive layer 14 (Figure 2) on the substrate 10. In addition, the component includes conductors 16 (Figure 2) on the substrate 10, and a semiconductor die 20 (Figure 2E, 3A or 7) in electrical communication with the conductors 16. The die 20 can be "flip chip" mounted as shown in Figure 2E, or "wire bonded" as shown in Figure 3A.

Each conductor 16 is defined by a pair of laser machined grooves 15 (Figure 2) in the conductive layer 14. As shown in Figure 2C, the conductors 16 comprise portions of the conductive layer 14 separated by the grooves 15, and by remaining portions of the conductive layer 14. As shown in

Figure 4, the grooves 15 are laser machined using a laser 44 and a base 48 configured to move the substrate 10 in X and Y directions.

In addition, as shown in Figure 2, each conductor 16 includes a bond pad 18 (pads or contacts in the claims) configured for flip chip mounting or wire bonding the die 20. Each conductor 16 can also include a contact pad 22 (contacts in the claims) configured for electrical connection to outside circuitry. In the case of wire bonding, an opening 40 (Figure 3A) can be laser machined in the conductive layer 14 for attaching the die 20 to the substrate. As shown in Figure 5A, the substrate 10BGA can also include conductive vias 58 in electrical communication with the conductors 16BGA, and contact balls 66 in electrical communication with the conductive vias 58.

ARGUMENT

The primary issue is whether claims 25-39 and 47-53 are unobvious under 35 U.S.C. 103(a) over Hembree et al. (US Patent No. 5,783,461) in view of Frankeny et al. (US Patent No. 5,065,227) and Pedder (US Patent No. 5,717,245).

The Examiner has held that independent claims 25, 30, 35, 47 and 52 do not patentably distinguish from the cited art as the limitation "laser machined grooves" has been given no significance. As stated in the Office Action: "an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not".

However, Applicant would argue that the product is unobvious over the art. In this regard, the limitation "laser machined grooves" describes a particular feature of the component, rather than a process for fabricating the component. The laser machined grooves permit the conductors to be smaller and more precisely dimensioned than conventional conductors formed by etching or deposition

processes. As stated on page 9, lines 12-13 of the specification: "A representative width W and spacing S can be as small as about 5 μm." In order to further distinguish the claims, this limitation has been added to amended independent claims 25 and 35.

Further, in assessing unobviousness, the claims should be read "as a whole" and this limitation should be considered in the context of the remainder of the claim. In this regard, independent claim 25 also recites a "conductive layer", and states the conductors comprise "portions of the conductive layer electrically isolated from one another by the grooves and separated from one another by remaining portions of the conductive layer". Independent claims 25, 30, 35, 47 and 52 recite similar limitations wherein conductors are defined by a conductive layer and grooves in the conductive layer.

In Figure 2C of the present application portions of the conductive layer 14 form the conductors 16, and portions of the conductive layer 14 separate the conductors 16. In addition to physically separating the conductors, the remaining portions of the conductive layer protect and rigidify the substrate 10.

In comparison, in Figure 1 of Hembree et al. the conductors 40 are the only conductive material that remains because they are formed by a metallization and sintering process (column 5, line 63, to column 6, line 1, of Hembree et al.). In Frankeny, metal 98 in Figure 5 are not portions of a conductive layer that has grooves defining conductors. Rather, the metal 98 forms electrically isolated and ground plane vias (column 6, lines 6-8), and circuitization is accomplished by traditional plating, photoimaging and etching techniques (column 6, lines 2-4). In Figure 9 of Pedder microstrip trimming stubs 94, 95 are formed in a metallization layer that includes a ground plane 80 (column

8, lines 46-48). The ground plane 80 is in effect another conductor rather than a metal separation layer formed by laser machined grooves.

Another feature not disclosed by the cited art is that the laser machined grooves also form bond pads 18 (Figure 2) for wire bonding or flip chip mounting the die, and contacts 22 (Figure 2) adapted for connection to outside circuitry. Independent claims 30 and 52 recite the bond pads for the die. Independent claim 47 recites the bond pads (first contacts) for the die, and the contacts (second contacts) for the outside circuitry. Again the bond pads and the contacts can be smaller and more accurately formed by the laser machined grooves.

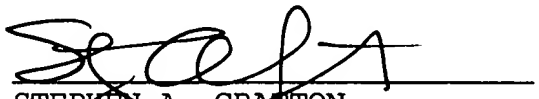
In view of the above features which are not disclosed by the prior art the amended claims "taken as a whole" are submitted to be unobvious over the prior art.

Conclusion

In view of the above amendments and arguments, favorable consideration and allowance of claims 25-39 and 47-53 is requested. Should any issues remain, the Examiner is asked to contact the undersigned by telephone.

DATED this 29th day of April, 2002.

Respectfully submitted:



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Marked Version Of Specification Showing Location of Changes

25. (thrice amended) A semiconductor component comprising:

a substrate having a first surface and an opposing second surface;

a conductive layer on the first surface;

a plurality of conductors on the first surface defined by a plurality of laser machined grooves through the conductive layer, the conductors comprising portions of the conductive layer electrically isolated [from one another] by the grooves and separated [from one another] by remaining portions of the conductive layer, the conductors and the grooves having a width as small as about 5 μm;

at least one semiconductor die on the first surface in electrical communication with the conductors;

a plurality of conductive vias [through] in the substrate from the first surface to the second surface in electrical communication with the conductors; and

a plurality of external contacts on the second surface in electrical communication with the conductive vias.

26. (thrice amended) The semiconductor component of claim 25 [further comprising] wherein the conductors comprise a plurality of pads [on the conductors bonded to] and the semiconductor die is wire bonded to the pads.

27. (thrice amended) The semiconductor component of claim 25 [further comprising a plurality of pads on the conductors and] wherein the semiconductor die is flip chip mounted to the [pads] conductors.

28. (twice amended) The semiconductor component of claim 25 wherein the substrate comprises a material selected

from the group consisting of plastic, glass filled resin, silicon, [and] ceramic, metal, germanium, and gallium arsenide.

29. (twice amended) The semiconductor component of claim 25 wherein the conductors comprise a plurality of contacts adapted for electrical connection to outside circuitry.
[external contacts comprise balls in a grid array.]

30. (thrice amended) A semiconductor component comprising:

a substrate having a surface;

a conductive layer on the surface having a thickness;

a plurality of conductors and pads on the surface defined by a plurality of pairs of laser machined grooves through the thickness of the conductive layer extending on the surface in a first direction and in a second direction, each conductor and each pad comprising a portion of the conductive layer [which is] electrically isolated [on either side by a pair] by a plurality of laser machined grooves; and

a semiconductor die flip chip mounted to the pads.
[on the surface in electrical communication with the conductors.]

31. (twice amended) The semiconductor component of claim 30 further comprising a plurality of contacts on the conductors adapted for electrical connection to outside circuitry.
[laser machined opening in the conductive layer configured for mounting the semiconductor die to the substrate.]

32. (twice amended) The semiconductor component of claim 30 further comprising a plurality of conductive vias in the substrate in electrical communication with the conductors

and with a plurality of contact[s] balls on a second surface of the substrate.

33. (twice amended) The semiconductor component of claim 30 wherein the component comprises a chip module, a multi chip module or a package.
[semiconductor die is flip chip mounted or wire bonded to the conductors.]

34. (twice amended) The semiconductor component of claim 30 further comprising an encapsulant at least partially covering the semiconductor die and at least a portion of the surface.

35. (thrice amended) A semiconductor component comprising:

a substrate having a surface;

a conductive layer on the surface;
[having a thickness;]

a plurality of conductors on the surface comprising portions of the conductive layer, [each] the conductors defined and electrically isolated by a [pair] plurality of laser machined grooves through the conductive layer, each conductor having a width and each groove having a spacing as small as about 5µm; and

a semiconductor die on the substrate in electrical communication with the conductors.
[;]

[with the thickness of the conductive layer, and a width of the conductors selected to provide a selected impedance for the conductors.]

36. (twice amended) The semiconductor component of claim 35 further comprising an encapsulant at least partially

covering the semiconductor die and at least a portion of the surface.

37. (twice amended) The semiconductor component of claim 35 wherein the conductors comprise pads bonded to the die and contacts adapted for electrical connection to outside circuitry.
[further comprising a plurality of conductive vias in the substrate in electrical communication with the conductors and with a plurality of external contacts on a second surface of the substrate.]

38. (twice amended) The semiconductor component of claim 35 wherein the substrate comprises [silicon] a semiconductor material and an electrically insulating layer on the surface.

39. (twice amended) The semiconductor component of claim 35 wherein the substrate comprises a material selected from the group consisting of plastic, glass filled resin, [and] ceramic, silicon, metal, germanium, and gallium arsenide.

47. (thrice amended) A semiconductor component comprising:

a substrate having a surface;

a conductive layer on the surface; and

a plurality of conductors on the surface defined by a plurality of [pairs of] laser machined grooves through the conductive layer extending in a first direction or a second direction on the surface, the conductors comprising portions of the conductive layer which are electrically insulated from one another by the laser machined grooves, the portions of the conductive layer including first contacts on first ends thereof configured for bonding, and second contacts on second

ends thereof configured for electrical connection to external circuitry; and

a semiconductor die on the substrate bonded to the first [pads] contacts.

48. (amended) The semiconductor component of claim 47 wherein the semiconductor die is flip chip [bonded] mounted or wire bonded to the first contacts.

49. (amended) The semiconductor component of claim 47 wherein each conductor has a first width of about 5 μm. [the semiconductor die is wire bonded to the first contacts.]

50. (amended) The semiconductor component of claim 47 wherein each groove has a second width of about 5 μm. [the component comprises a chip module, a multi chip module or a package.]

51. (amended) The semiconductor component of claim 47 wherein the conductive layer [comprise a laser machined] includes an opening for attaching the die to the substrate.

52. (twice amended) A semiconductor component comprising:

a substrate having a surface;

a conductive layer on the surface;

a plurality of conductors on the surface defined by a plurality of first laser machined grooves through the conductive layer to the surface, the conductors comprising portions of the conductive layer electrically isolated [from one another] by the grooves and separated by remaining portions of the conductive layer;

a plurality of contacts on the conductors defined by a plurality of second laser machined grooves through the conductive layer to the surface;

a plurality of conductive vias through the substrate in electrical communication with the conductors; and

a semiconductor die on the substrate in electrical communication with the contacts.

53. (amended) The semiconductor component of claim 52 further comprising a plurality of contact balls on the substrate in electrical communication with the conductive vias and arranged in a ball grid array.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8

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April 29, 2002
Date of Signature

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